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LOW POWER TEST PATTERN GENERATION USING TEST-PER-SCAN TECHNIQUE FOR BIST IMPLEMENTATION

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ABSTRACT

This paper introduces the function of test cases with minimal power for Built-In-Self-Test (BIST) implementation. This method intends Test-Per-Scan (TPS) based test cases using Multiple Single Input Change (MSIC) architecture. Multiple SIC patterns are developed by using EX-OR operation of twisted ring counter and test design algorithms like Linear Feedback Shift Register (LFSR),Bit-Swapping LFSR (BSLFSR), and Cellular Automata (CA). These patterns are used to a diminish number of transitions in the test patterns that are generated. The preferred method uses Test-Per-Scan technique for generating Multiple SIC test patterns. TPS diminished the power consumption during test mode. The seed generator used in TPS is modified LFSR's i.e., BS-LFSR, Cellular Automata (CA). BS-LFSR is composed of with an LFSR with a multiplexer. In CA, it also presents a variation on a BIST technique, which is from a one-dimensional cellular automaton; the pseudo random bit generator is generated. The proposed Hybrid Cellular Automata (HCA) using the rules 90 and 150 to generate the pseudo random designs. Moreover, the CA implementations illustrates properties of data compression like LFSRs and that they exhibit locally and with topological consistency significant attributes for a VLSI design. In this proposed method, LFSR is replaced with BS-LFSR, and HCA. Simulation and synthesis outcome with ISCAS c432 benchmark determine that Multiple SIC can reduce the power consumption.

Index Terms: BIST, MSIC, LFSR, BSLFSR, CA, HCA, circuit under test, test-per-scan, single input change, test response analyzer, pseudo random generator.

1. INTRODUCTION

Built-In-Self-Test scheme can adequately minimize the more complex VLSI analysis problems, by generating test hardware into the Circuit-Under-Test (CUT). The Linear Feedback Shift Register (LFSR) is generally exploited as Test Pattern Generators (TPGs) and Test Response Analyzers (TRAs) in traditional BIST technique. Amainsnag of these techniques is that the pseudorandom test cases produced by the LFSR causes a notably huge switching activity in the CUT, which can lead to enormous power dissipation and also blow the circuit and reduce the product yield. The LFSR generally requires very lengthy pseudorandom patterns in order to attain the required fault coverage in BIST implementation.

A. History work on BIST

There are a number of contrives that are used to generate design necessary for testing CUT. It has been founded that power consumption is more in test mode comparatively with normal mode [12]. The main idea behind low power techniques is to minimize the power consumption in test mode. Different kinds of test generation methods are required to develops table Built-In Self-Test (BIST) techniques. The utmost familiar test pattern design generation is based on pseudorandom pattern generators (PRPGs). The simple hardware on-chip test generation can be developed by pseudorandom tests patterns. Therefore, there are two major forms of PRPGs which is derived. Generally, the linear feedback shift registers and 1- Dimensional (1-D) Linear Hybrid Cellular Automata (LHCA) are major forms of PRPGs.

In spite of few coincidences, the series of states is consistently distinct between the LHCA and the LFSR, the LHCA can generates far good randomized test patterns [21]. The CA-based test generators will be an option to traditional LFSR algorithms. Further to meliorated randomization attributes, novel pseudorandom test design algorithms also have benefit in that they can be implemented for only contiguous neighbor communication and the physical length of the pattern generator. These can be elevated or diminished by only summate or deducting the cells. However, the investigation of aliasing function is a secondary controllable job for the CA than LFSR. The architecture in [7], presents Seeded Autonomous Circular Shift Register (SACSR) producing Single-Input-Change (SIC) patterns of maximum unique vectors. One of the ways to minimize power consumption is by reducing the transitions between the consequent patterns. Many techniques are introduced to minimize the transitions. The architecture in [3] presents Bit Swapping LFSR which is unlike from conventional LFSR reduces 33% of the transitions. BIST technique should generate test sequences with shallow power and area overhead and high fault coverage.

The architecture in [8] the introduced method has to decrease scan input bit transitions along operations of scan shifting. The architectures in [9], [11], [13] introduced various new techniques for reducing switching activities and also area overhead. The architecture in [2] introduces a new technique for generating the test designs with only single bit change compared with the previous patterns and generated using the XOR of the counter output with LFSR. The architecture in [5] power is